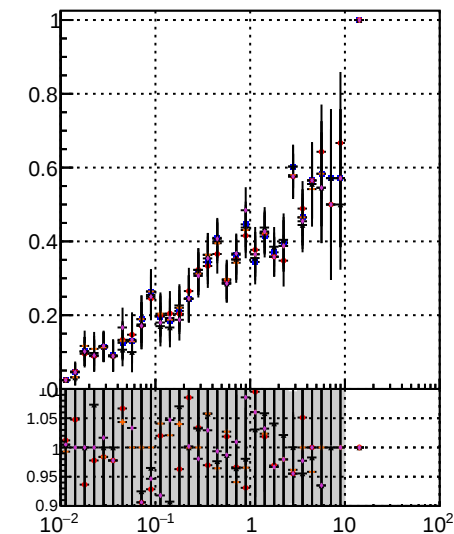


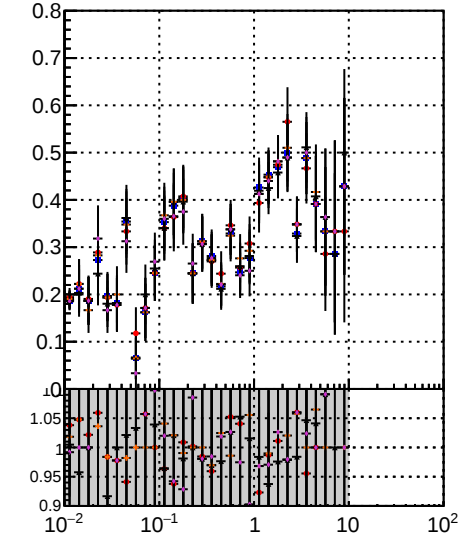
Fake rate vs vertpos



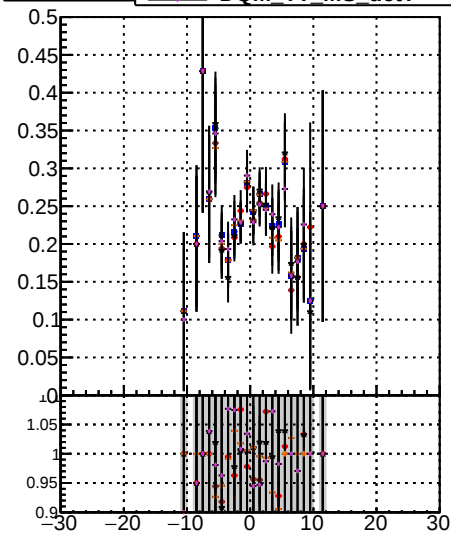
Duplicates Rate vs vertpos

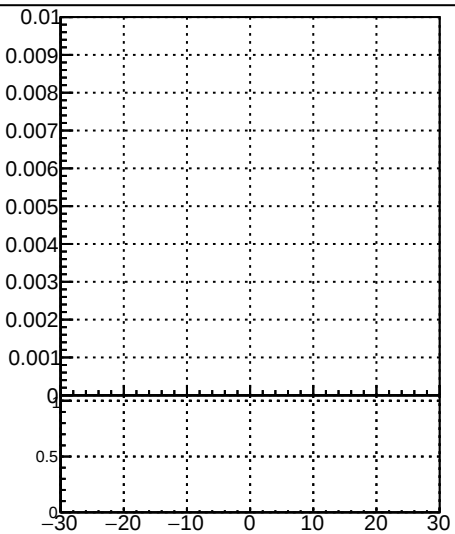


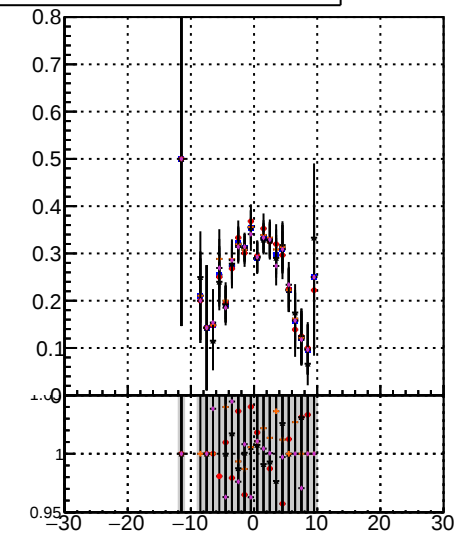
Pileup rate vs vertpos



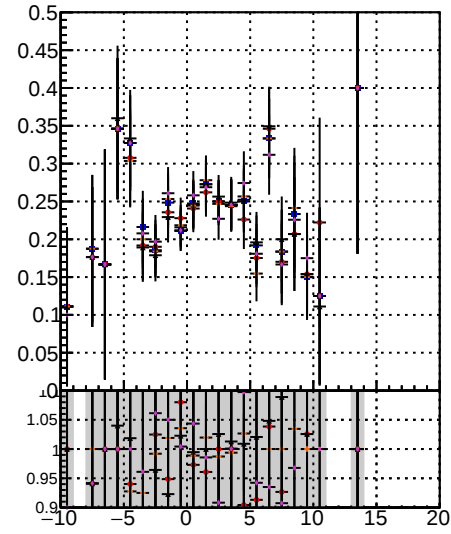
The diagram illustrates the system architecture. It starts with a box labeled "Fake rate vs v". This box is connected to a central processing unit represented by a rectangle with horizontal lines. To the right of this unit is a vertical stack of four boxes labeled "DOM", "TT", "MS", and "init". These boxes are connected to a final output box labeled "def".



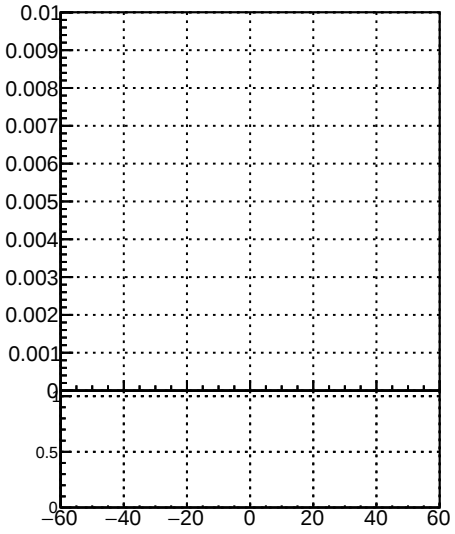




Fake rate vs. sim PV z



Duplicates Rate vs sim PV z



Pileup rate vs. sim PV z

